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A Comprehensive Study on Utility of Carrier Transportation Layer for Efficiency Improvement of Organic Photovoltaic Devices using GPVDM Modeling

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ABSTRACT

A well-prepared abstract enables the reader to identify the basic content of a A comparative study on the electrical parameters of organic photovoltaic device has been taken into consideration for unified realization about the need of carrier transportation layer in organic photovoltaic devices. The parameters have been measured by modeling the devices using simulation technique. Device efficiency of transportation layer P3HT:PCBM incorporated device has been obtained increasing comparatively. Possible reason of such improvement in device efficiency has been demonstrated on the basis of theoretical point of view. Series resistance and ideality factor has been estimated from IdV/dI-I plot. About three times reduction of the following has been encountered with addition of P3HT:PCBM compound. Such significant reduction of series resistance (Rs) and trap energy (Et) are found to be responsible for the probable reason of improvement of device efficiency which are calculated by analyzing Current-Voltage (I-V) characteristics. Differential technique of current voltage relationship has also been implemented to explain the trapping distribution for both devices. It has been found that trap factor increases for P3HT:PCBM compound device comparatively which concludes better conduction into the device.

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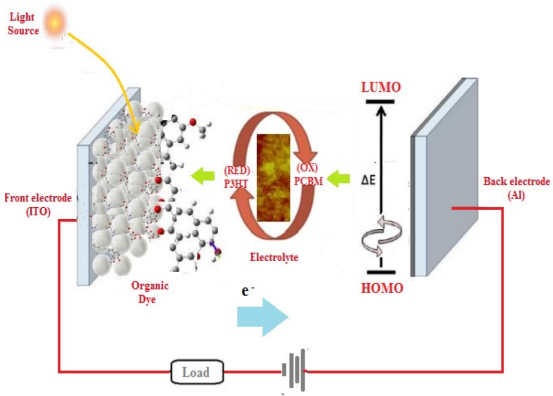
1. INTRODUCTION

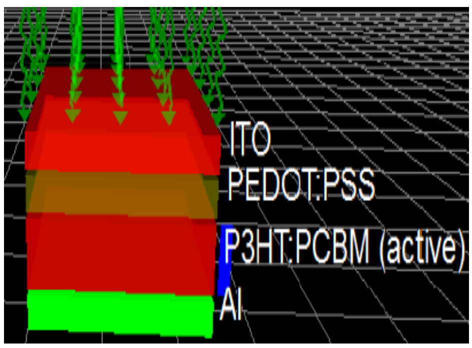
The organic dye based solar cells have been receiving hot debated concern over last few years. Flexibility, light weight, availability of herbal ingredient, easy preparation technique of samples provides extra advantage to its utility as alternative way of conventional materials for formation of such devices [1-2]. Though the application of this kind of devices is convincing as well as interesting enough but some fundamental limitations still it is facing in improving its efficiency. Incorporation of different nano-particles, nano-tubes, nano-ribbons with active organic layer, application of electrolytes have been introduced to find out the solution of efficiency improvement. Outcome of present experimental modeling shows consistency with numerous previously reported such attempts. Moreover, the physics of photo conversion efficiency (PCE) enhancement with insertion of electron transportation layer along with photoactive layer has been described. In this regard, the fact of realization should be started from the illustration of dark current-voltage (I-V) curve of the diodes, which shows linearity in semilog range of measurements below threshold voltage. But the characteristic deviates from linearity with increasing bias voltage. Presence of series resistance is one of the most significant factors which basically results this deviations [3]. Since absorbance of organic thin films is high enough and excitons dissociation process is very fast for dissociation efficiency to achieve unity, the performance gradually becomes limited by short exciton diffusion length and very low charge collection due to high value of series resistance. Even series resistance of the bulk region of the film resists photo generated charges at the level of donor-acceptor interface from reaching to the electrode. In the bulk region traps play an important role in the carrier conduction process. At below threshold voltage region of I-V curve, effect of trap is negligible and current exhibits ohmic nature. Charge injection at this regime is too low and transport mechanism is explained by well-known Mott-Gurney's equation. Influence of trap on I-V characteristics can be understood above threshold voltage regime. Majority of generated charges face immobilization of motion due to the reason of trap existence above threshold voltage regime [4]. Such trapping states create an internal resistive property of organic substances. So it is obvious that the movement of free carriers of these devices struggles by high series resistive influence due to the presence of trapping states in the active regime. Investigation of the present report suggests that both of Rs and Et has been reduced with incorporation of blend composite of P3HT:PCBM with active material through which charges will be passed. Lowering of trap energy inherently lowers the influence of Rs which is the reason of enhancement of fill factor as well as efficiency of the solar cell.

2. Numerical Modeling and Experiments

GPVDM (General Purpose Photovoltaic Device Model), a very renowned, recently updated and reliable simulation modeling technique [5-6], has been introduced for current research to understand the physics of the charge transport mechanism and measurement for comparison of electrical as well as photovoltaic parameters of single and bi-layer photovoltaic devices. This modeling technique brings a revolution in research of organic photovoltaic devices by providing numerous advantages like device characterization by analyzing simulation outcome, ease programming of device modeling, prediction of improved device designing and its application and realization of charge conduction physics in organic photovoltaic devices finally. Numbers of typical relevant parameters have been taken into account to execute GPVDM successfully (given in supplementary file). Active layer of the experimental devices is considered to be sandwiched between the front and back electrodes. Thickness of the active layer is a very important issue on which device efficiency basically depends [7]. If active semiconductor layer regime is thin enough then efficiency is found to be low because of less absorption of photon whereas with enhancement of layer thickness leads to recombination of photo-generated carriers before reaching polymer/heterojunction interface which is unintended for improvement of efficiency. It has been observed that device performs better between thickness range 200nm-250nm [5, 16]. The devices under experiment have been performed considering layer thickness 220nm in this work. I-V characterization has been simulated and the data has been extracted using Graph extractor and plotted accordingly. Series resistance (Rs) of the devices has been determined theoretically by analyzing IdV/dI-I plot whereas trap energy (Et) has been estimated from log I-V characteristics. From outcome of simulation modeling, photovoltaic parameters has been extracted and compared for both type of devices. The only photoactive layer (PAL) based device is abbreviated as PALD and electron transport layer (ETL) added with PAL is named as ETLD.



(a)



(b)

Figure 1. Block diagram representation of organic dye based photovoltaic measurement setup (a) in experiment and (b) in GPVDM simulation

3. RESULTS AND DISCUSSIONS

Output of simulation indicates that the effectivity of electrical parameters as well as device efficiency is improved enough for bi layer device. To have a better insight of the result, current-voltage (I-V) characteristics have been taken into account. Evaluation of the data shows that current has considerably increased for ELTD. The following I-V characteristic is shown in Fig.2.

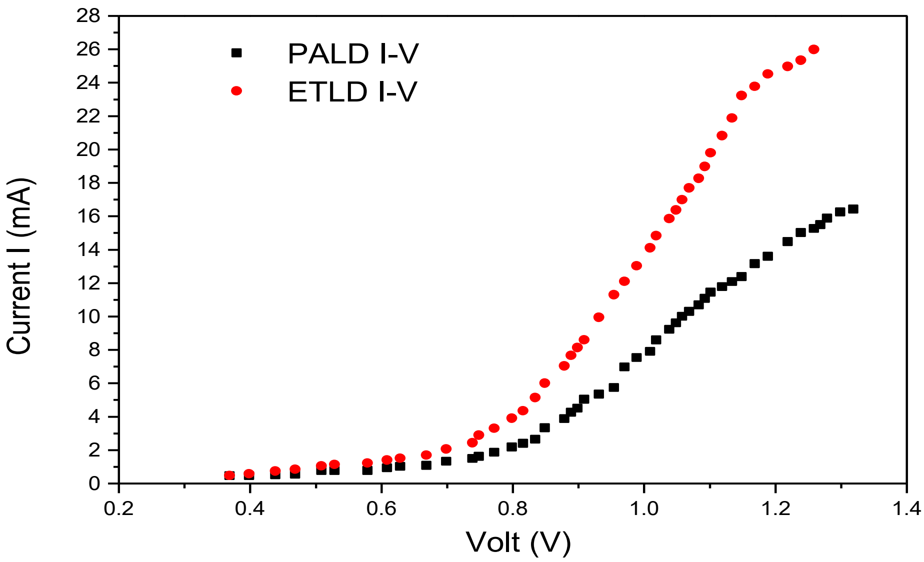


Figure 2. I-V characteristics of PALD and ETLD obtained in GPVDM (plotted in origin 5.0)

There are various factors actually affecting the current conduction procedure of organic device. But the factor has the major impact on the conduction of carriers is termed as Rs. The parameter is considered as a crucial reason of non ideal behavior of organic devices. Rs directly impacts on fill factor and explicitly on device efficiency. Therefore, device efficiency is expected to be improved with decrement of the parameter Rs. In order to estimate Rs, approach of estimation of the parameter deals with I-V characteristics using the formula of Rakhshani et al [8]. I-V characteristics for high value of Rs of photovoltaic device can be expressed by [8-10]:

$$I = I_0\left[e^{q(V-IR_s)} - 1\right] \tag{1}$$

Whereas voltage can be explained in terms of current as follows

$$V = \frac{nkT}{q}\ln\left(\frac{I}{I_0} + 1\right) + I\,R_s \tag{2}$$

Derivative of voltage with respect to current can be written as

$$\frac{dV}{dI} = \frac{nkT}{q}\frac{1}{\left(\frac{I}{I_0}\right)+1}\frac{1}{I_0} + R_s \tag{3}$$

Since current I is high enough than reverse saturation current I_0 (i.e., $I \gg I_0$) at the high current regime. So the Eq. (3) can be expressed as

$$I\frac{dV}{dI} = R_s I + \frac{nkT}{q} \tag{4}$$

From above consideration at high current zone, $I\frac{dV}{dI}$ is linearly dependent on total current I. R_s can be extracted from the slope by introducing a linear fit in the high current region whereas ideality factor n can be estimated from the intercept of the linear fit using Eq. (4). Dark I-IdV/dI characteristics for both devices are shown in Fig. 3.

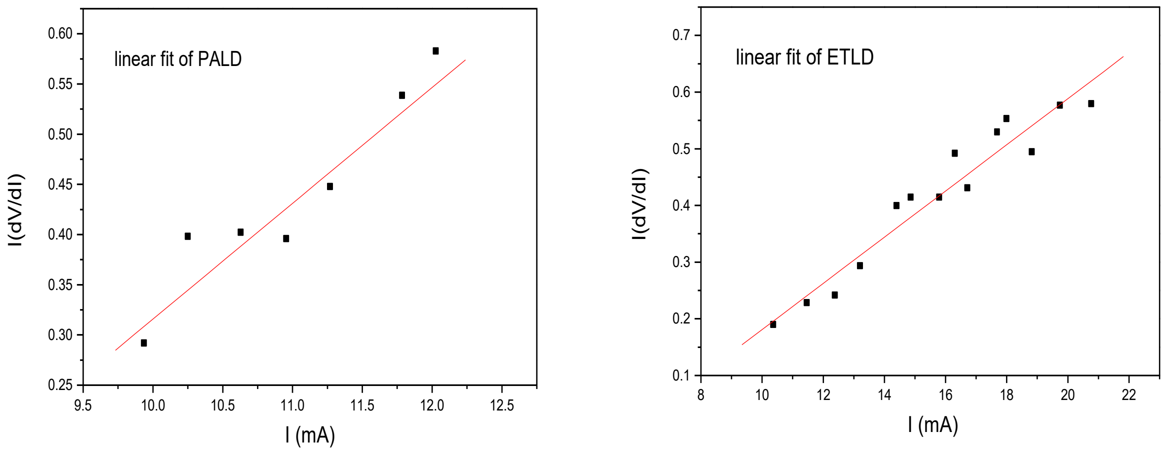


Figure 3. $I\frac{dV}{dI}$ vs I characteristics of PALD and ETLD

n is such a parameter which indicates the tendency of linearity of ideal diode. The value of n is usually very high in organic devices due to the distortion of current-voltage characteristics generated by interfacial disorder, mismatch in metal-semiconductor interface, hopping carrier transport and high series resistive impact [10, 32]. It has been found that the value of ideality factor reduces drastically with insertion of charge transportation layer based ETLD. Rs is closely related also with another important parameter, named as Trapping effect which has high influence on organic photovoltaic devices. Presence of significant concentration of trapping states becomes a factor in organic semiconducting devices which appears due to the disordered elementary structures of organic molecules and has a significant contribution to produce high value of Rs. The role of trap is a matter of concern in carrier conduction mechanism of organic dye based devices [4, 10, 19]. Charges interact with these traps when conduction occurs. Injected carriers depend on the trap energy for a particular distribution. For bulk transport process, it is a vital function which controls current flow by providing resistive influence. Basically charges are trapped and recombined in presence of huge amount of traps concentration. Hence conductivity gradually becomes limited which gradually results low device efficiency. Existing trap concentration deliberately adds resistive impact which prevents smooth flow of the carriers into bulk transport regime. It has been observed in present experiment that incorporation of a polymer layer (P3HT:PCBM) which acts as interfacial electron transportation layer with PEDOT:PSS reduces the amount of trap energy Et in ETLD. It will be rather convenient to describe the fact from Fig. 4.

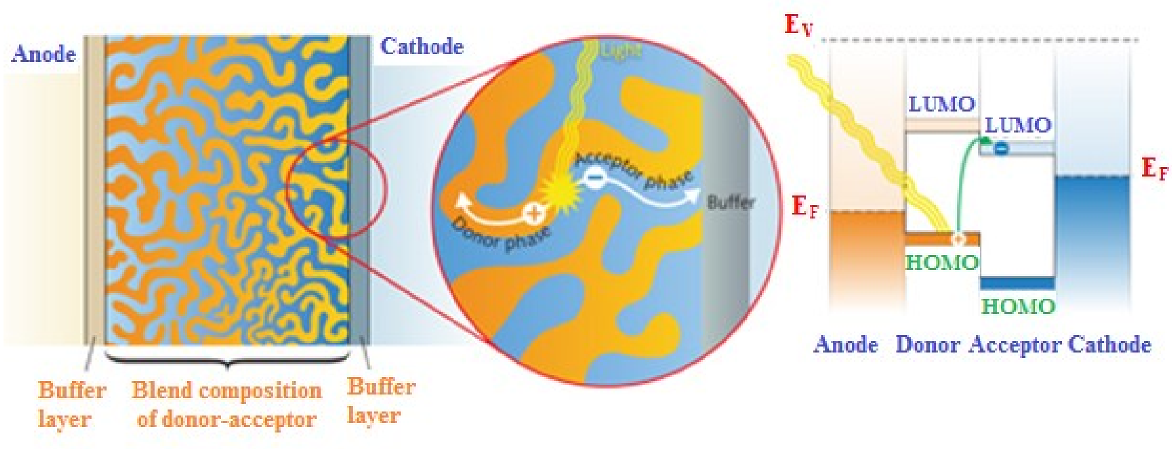


Figure 4. absorption of photon energy generates dynamic holes and electrons that travel through acceptor and donor phases and its consequent energy level diagram where E_v represents the energy at vacuum level and E_F expresses the energy of Fermi level [6, 28, 31]

Electrons move from highest occupied molecular orbital (HOMO) of donor molecules towards lowest unoccupied molecular orbital (LUMO), leaving a positive carrier "hole" on donor molecule during absorption of photon energy. Holes and electrons move along opposite directions together and simultaneously captured by anode and cathode [4, 24-26]. The interfacial transition between electrode and organic dye is critical enough for efficient collection of carriers. Such charge transformation causes significant drop of voltage and moreover, leakage current impact on electrodes, resulting decrement of PCE. Incorporation of charge transportation buffer layer (P3HT: PCBM) in ETLD, plays crucial role to minimize the effect of voltage drop and leakage current. The layer permits interfacial alignment of energy-level providing rectification and additional percolation network to trapped charges and on the other hand, absorption of more optical energy by this layer results comparatively greater range of free carriers [10-27-28]. Increasing tendency of free carrier concentration reduce the energy of trapping states and hence series resistance also. Moreover, insertion of buffer layer in ETLD results high value of Jsc and Fill factor (FF) which inherently improve the device efficiency comparatively than PALD [4, 29]. Carrier transportation buffer layer acts as a bridge between the work function differences to provide suitable charge transport into the bulk region which seems to another probable reason of reduction the trapping states consecutively. Fig. 5 can be effective in this regard to show the charge hopping mechanism on the basis of work function of materials [5, 20-22] into the device. Fermi level energy of materials are parameterized by their work function [11, 25-26]. Work function determines the amount of energy loss when removing or adding an electron from a substance. Maximum value of open circuit voltage (Voc) can be found with greater value work function of anode over ionization energy of donor atoms and low value of cathode work function than acceptor electron affinity [7, 23-24].

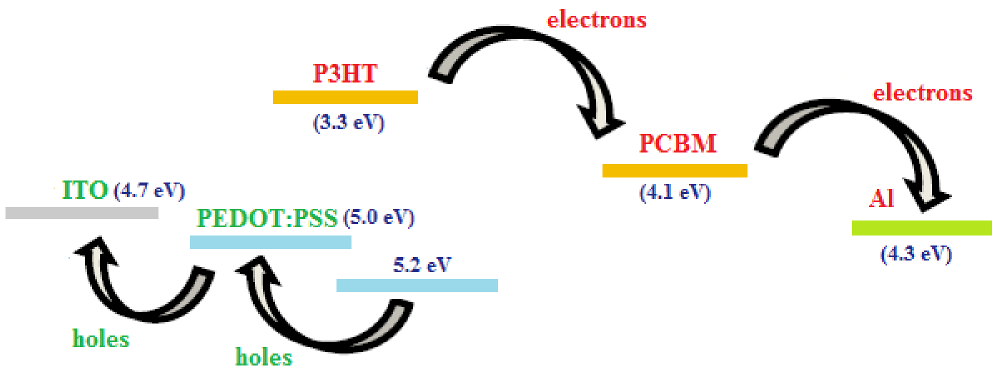


Figure 5. hopping movement of carriers in different materials as par work function into ETLD

Exponential distribution of trapping concentration and its solution relates current density and applied voltage in such a way that they maintains the following relation $J \sim V^{m+1}$, where $m = {}^{T_c}/_{T}$, T_c is the characteristic temperature and T is room temperature and Trap energy $E_t = mkT$. Value of m is calculated from lnI-lnV plot and hence E_t is extracted from the value of m using the relation mentioned above [4, 11]. Trapping carrier concentration (n_t) can be explained by exponential distribution as follows [12, 19]

$$n_t(\epsilon) = N_0 \exp \frac{-\epsilon}{kT_c} \tag{5}$$

where ∈ expresses the traps depth below conduction band mobility regime and T_c is the trap energy of the following distribution. Impact of trapping on I-V characteristics can be described from the modified version of well known Mott-Gurney relation and is given by [13]

$$I = \frac{9}{8} A \,\epsilon\epsilon_0\, \theta\mu \frac{(V-V_x)^2}{d^3} \tag{6}$$

where V is applied voltage, ϵ_0 is free space permittivity, μ is carrier mobility, d is thickness of the semiconducting and θ is trap factor. Values of θ can be estimated from logarithmic representation of I-V plot. θ has significant signature about the indication of improvement of trapping states. Aforementioned parameter denotes the ratio of the amount of trapped charges (P_t) to total number of free charges participated in conduction process (P_f) as well as the trapped charges and can be represented as [13-14]

$$\theta = \frac{P_t}{P_f + P_t} \tag{7}$$

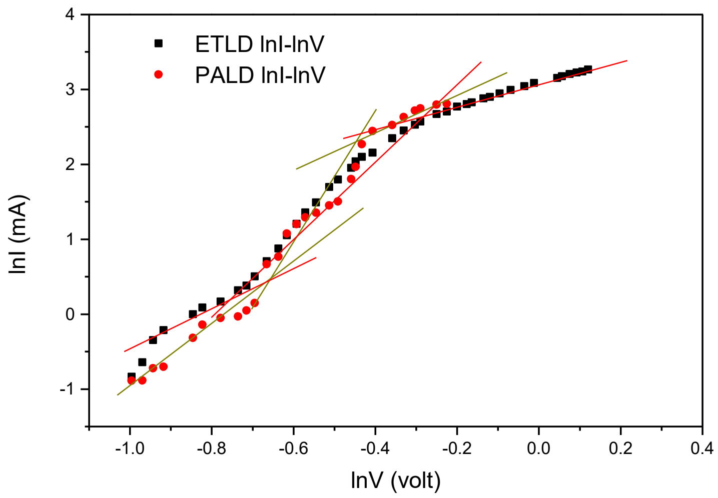


Figure 6. InI-lnV characteristics of PALD and ETLD

To have a better insight about the trapping distribution into the devices a differential technique should be implemented. Distortion in I-V curve is clearly observed in presence of large trap concentrations and distinct regions containing distortions can be unambiguously predicted. But the prediction becomes quite problematic to recognize the distortions in the plot for low trap density. Differential technique is fruitful in this context for enhancement of the small deviations so it has been introduced to reveal the orientation of distribution of trap states. G(V)-V plot is explained regarding this purpose where [12,15]

$$G(V) = \frac{d\log(I)}{d\log(V)} \quad (8)$$

A transition of exponentially rising current flow to power law dependence regime about built in potential voltage (Vbi) is marked by sharp peak of G(V). Filling of trap states can be illustrated by such peak which signifies easy identification of transition voltage related to voltage Vbi. The distinct peak of G(V)-V curve explains the nature of trapping distribution where monotonous decrement from sharp peak of G(V) with increasing voltage denotes the trap free conduction into the device.

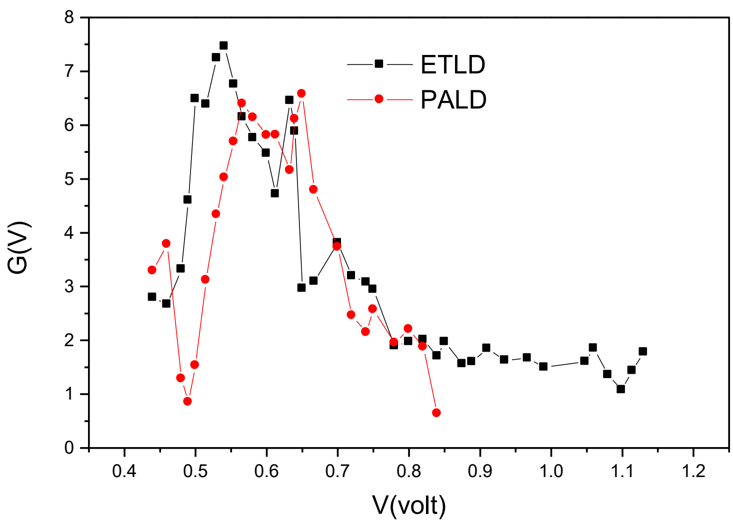


Figure 7. G(V)-V characteristics of PALD and ETLD

Exponential behaviour at power law regime with sharp peaks are noticable clearly for both devices in Fig.7. Sharp peak of G(V) indicates the change in slopes from exponential regime to power law regime as mentioned earlier. Decrement of trapping density can be clearly concluded with comparatively greater monotonic decremental orientation of G(V) at high voltage for bilayer devices. Height of trap peaks depend upon the slope of current voltage relationship which can be measured by the variation of θ. Traps are progressively got filled with increasing voltage which leads to the enhancement of θ from its minimum value towards unity. A relatively smooth conduction procedure can be expected with increasing value of θ. ETLD comprises of two distinct organic layers in which one layer having high ionization potential and electron affinity acts as acceptor while the other layer acts as donor of excitons. Electrostatic force arises in such configuration is strong enough to break the exciton pairs much efficiently than PALD. The thickness of acceptor layer is ranged in such a way that large amount of photons are absorbed and transported through acceptor successfully [16]. In this process, amount of recombination is comparatively small than PALD configuration so greater range of charge can be transported from one electrode towards another. Improvement in carrier conduction is caused by low value of trapping energy. Since organic structures are disordered and prone to traps, they usually have high resistive impact. The trapping problems can be optimized by the insertion effective polymer layer which leads to reduction of series resistance also and electrical parameters as well as device efficiency enhances gradually.

Table 1. Comparison of electrical parameters of PALD and ETLD

Electrical parameters	**PALD**	**ETLD**	**% improvement in ETLD**
Trap Energy, E_t (in eV)	0.040	0.014	65.0
Series resistance, R_s (in Ω)	115	40	65.2
Ideality factor	30.88	8.73	71.7
Trap factor, θ	0.275	0.342	24.4

Photovoltaic parameters have been obtained from the output result of simulation technique. Obtained values of the parameters have been given in Table 2. Efficiency of solar cell (ɳ) can be defined as ratio of maximum power of the device to the power of incident photons and is expressed as [4, 17-18]

$$\eta = \frac{J_{sc} \times V_{oc} \times FF}{\emptyset} \times 100 \quad (6)$$

where $\emptyset$ is intensity of incident photons, Jsc is short circuit current, Voc is open circuit voltage and FF is fill factor of the device. FF can be estimated from the following relation

$$FF = \frac{V_m \times J_m}{V_{oc} \times J_{sc}} \quad (7)$$

where Jm and Vm are maximum current density and voltage at maximum power rectangle.

Table 2. Comparison of photovoltaic parameters of PALD and ETLD

Photovoltaic parameters	**PALD**	**ETLD**	**% improvement in ETLD**
V_{oc} (V)	0.602	0.668	10.9
J_{sc} (A/m^2)	111.63	220.52	97.5
FF	67.11	74.19	10.5
ɳ (%)	4.51	10.93	142.9

The result shows consistency with the analytical illustration stated earlier and also with previously reported experimental outcomes [4, 32-36]. Fill factor is observed to increase in the ETLD due to less number of recombination and lower trapping concentration. Though Voc does not change significantly with insertion of ETL but a considerable increment of Jsc is observed in ETLD structure which suggests that photo generated carrier is enhancing with addition of that corresponding layer in the aforementioned device.

4. CONCLUSION

Improved device performance with insertion of semiconducting polymer layer between PEDOT:PSS and electrode has been explained. Electrical parameters like Et, Rs, n and θ are obtained from by analyzing different I-V characteristics for both devices. It has been found that electrical parameters are improved for ETLD. Trapping orientation has been demonstrated by introducing differential technique for both devices. Greater range of monotonic decrement of G(V) has been found better for bi-layer devices which leads relatively trap free smooth conduction at higher voltage regime. Photovoltaic parameters have been encountered for single and bi-layer devices respectively. Physics of the PCE of ETLD has been vividly illustrated. It has been observed that Jsc, fill factor is enhanced for ETLD structures with reduction of Rs as well as Et which is inherently the reason of device efficiency.

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COMFLICT OF INTERESTS

On behalf of all authors, the corresponding author states that there is no conflict of interest.

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